Implementation of Efficient Ternary Content Addressable Memory by Using Butterfly Technique

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Abstract: *A CAM is a device that used for search and store data and using comparison logic circuitry implements the table lookup function in a single clock cycle. CAMs are main application of packet forwarding and packet classification in Network routers [10]. A Ternary content addressable memory(TCAM) has three type of states '0','1' and 'X'(don't care) and which is like as binary CAM and has extra feature of searching and storing. The 'X' option may be used as '0' and '1'. TCAM performs high-speed search operation in a deterministic time. This type of devices power and speed are the important. So, in this work a TCAM circuit is designed by using butterfly match line (ML) Technique. The speed and power measures of the TCAM design and the experimental results show that outflow power may be reduced compared with the traditional TCAM design.*

Keywords: *Content Addressable Memory (CAM) Circuit, XOR-based conditional keeper, Ternary Content Addressable Memory (TCAM) Circuit, Pseudo-Footless Clock Data Pre-charge Dynamic Match line (PF-CDPD) Architecture.*

I. Introduction

Content addressable memory (CAM) is one type of memory the stored data is accessed by its contents and it's mainly used as search operation. This CAM divided into two types. Those are Binary CAM and Ternary CAM. The Binary CAM allows "0" and "1" s. And Ternary CAM is same like as Binary CAM but it can able to detect don't care state ("X"). TCAM allows read, write and search the binary values.

Ternary Content Addressable Memory (TCAM) is the useful for search and store ternary values and used for partial data matching. TCAMs are composition of conventional type semiconductor memory with addition of comparison circuitry. The most common application of TCAMs are packet forwarding and packet classification. The rest of this paper is organized as follows. Section 2 is the related work about butterfly match line technique. Section 3 is the proposed butterfly match line technique. Section 4 is the simulation results of the techniques. Section 5 is the conclusion of this paper.

II. Related work

Two widely used CAM cells are NAND-type and NOR type cells. Fig. 1(a) and (b) show an NOR-type cell and an NAND-type TCAM cell. The TCAM contain four important ports, Bit line is the use to write the value to SRAM. Data word line is used to control the NMOS. Search line is used to search the data and Match line is the output line it gives the result.

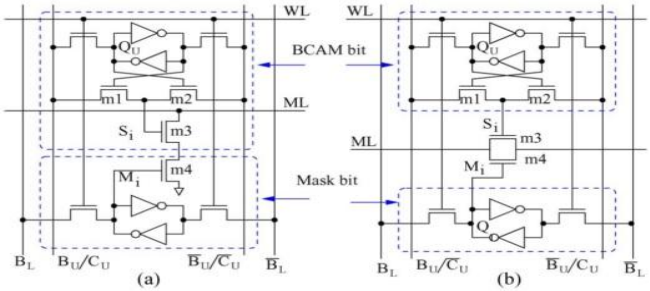

Fig. 1. (a) NOR-Type TCAM Cell. (b) NAND-Type TCAM Cell

TCAM have many existing methods in that NOR type match line method have high search speed but it have high power consumption and NAND type match line method have low power consumption but its performance is very low as compare than NOR match line. So, the disadvantage of NOR type TCAM is high power consumption and disadvantage of NAND type TCAM is search data speed is high.

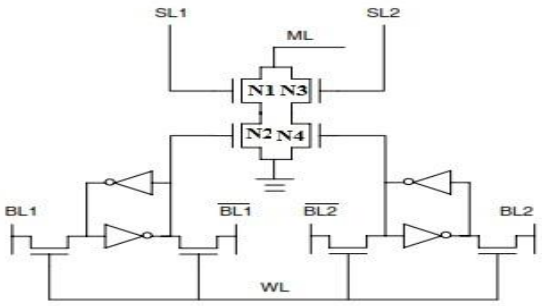

Fig. 2. Conventional TCAM

Figure (2) shows the conventional TCAM design using NOR based comparison logic and is quite common in use from a long time hence called conventional design. Here pair of transistors N1, N2 and N3, N4 forms a NOR type discharge path for the match line. It is called NOR type discharge path because discharge path of a CMOS NOR gate works in this fashion as if any of the inputs is 1 then NMOS corresponding to that input connect the output with ground. Here, ML is the output. TCAM Cell can be masked by switching off SL1 and SL2 i.e. SL1=SL2=0, which results in elimination of discharge path for already precharged match line.

This TCAM has three important operations, 1)Write: The binary values are write by using Bit line at that time the control bit act as on state.2)Read: The stored values are read by match line.3)Search: The values are search by using search line.

III. Software setup

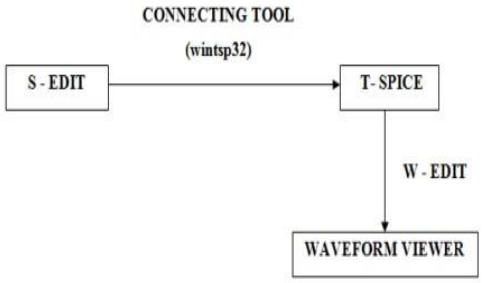

Fig. 3. Tanner software setup

S- Edit saves and reads design files in Tanner Research's proprietary S- Edit Database (SDB) format. An SDB file contains design information and setup information. S- Edit has two viewing modes: schematic mode and symbol mode. First schematic diagram draw in S-Edit and save it and Export it. Then open T-Spice tool by using wintsp32 application can be used to insert commands and files. Commands for adding voltage sources, transient analysis, input bit-stream and output constant can be done by using INSERT COMMAND tab. Once the program has been simulated without error, W-Editor can be used to analyze the waveform of given input and its corresponding output.

IV. Butterfly Match line Technique

The butterfly match-line (ML) TCAM scheme is proposed using pseudo-footless clock data pre-charge dynamic (PF-CDPD) structure. It is associated the each pipelined stage is in the butterfly association structure which is utilized for diminish the power consumption and search time.

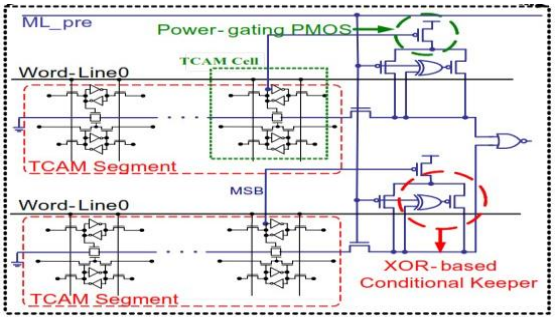

Fig. 4. Butterfly ML TCAM

The power utilization on the search line is reduced without any search time overhead. A noise-tolerant match-line (ML) scheme with XOR-based conditional keeper is introduced to diminish the power consumption and search time. With the specific end of the goal to reduce the search time overhead caused by butterfly connection style the XOR-based conditional keeper system can decrease delay of critical path of the match-line. Figure 4 shows the butterfly connection structure. The two CAM segments are associated in the butterfly connection structure. The two CAM segments are connected using two input NOR-gate, and controlled signal of next stage is generated by the two input NOR-gate output. The proposed butterfly match-line scheme with XOR-based conditional keeper gives the power saving and high performance.

V. Simulation Results

The Design and the implementation of the power reduction technique has been carried out in Tanner tool 13.0 version software tool of 0.18µm CMOS technology. The specifications that are followed in the simulation results are shown in the table 5.1. The most power consuming task is the search operation in the TCAM access. The Butterfly technique has been used to reduce power reduction and how far power and delay savings compare to traditional TCAM.

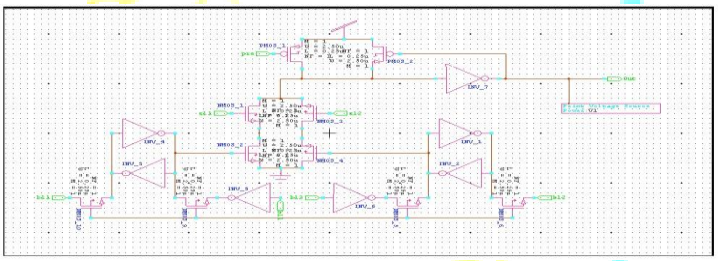

Fig 5.1(a) Circuit schematic conventional TCAM cell with comparison and storage parts

Figure 5.1(a) shows the Schematic conventional 4-bit TCAM cell. Here four TCAM cells are connected in series. Each TCAM cell has comparison logic and storage parts.

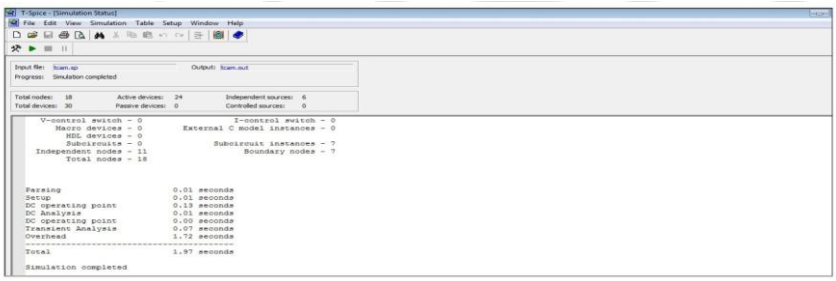

Fig 5.1(b) Speed analysis of Conventional TCAM

Figure 5.1(b) shows the Conventional TCAM Speed analysis. The speed obtained is 1.97 Seconds.

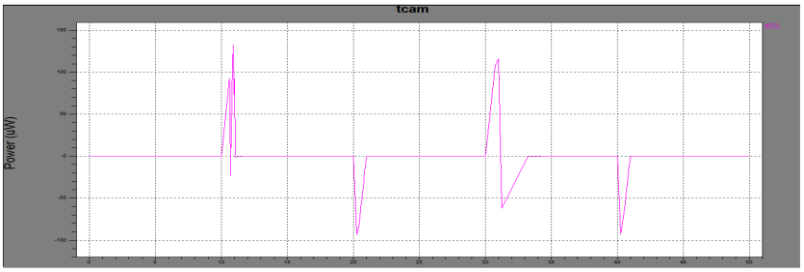

Fig 5.1(c) power analysis of Conventional TCAM

The figure 5.1(c) shows the power analysis conventional TCAM cell, which is used to compare the power reduced value to that of various implemented power reduction techniques. Here the power consumption obtained is 134µW.

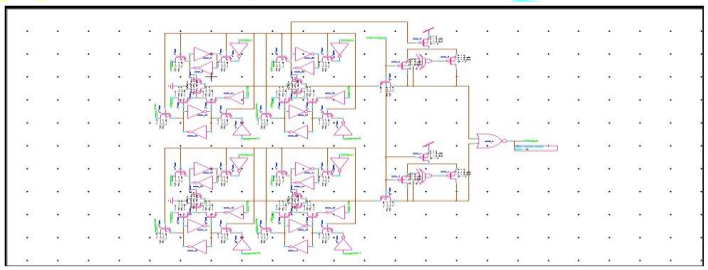

Fig 5.2(a) Circuit schematic of butterfly ML scheme

Figure 5.2(a) shows the butterfly match line scheme which is connected the TCAM segments are in pipelined architecture. Four TCAM segments are connected with NOR gate.

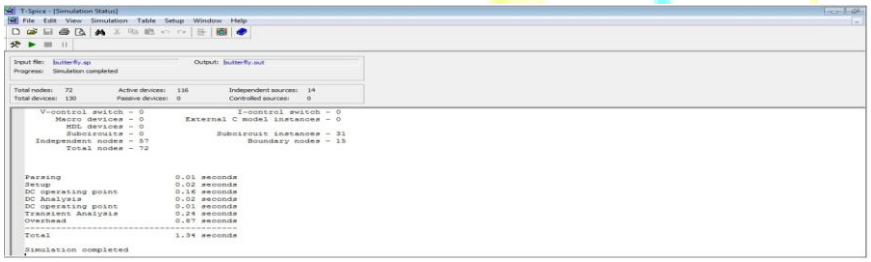

Fig 5.2(b) speed analysis of the butterfly ML scheme

Figure 5.2(b) shows the speed analysis of butterfly match line scheme and obtained speed is 1.34 Seconds.

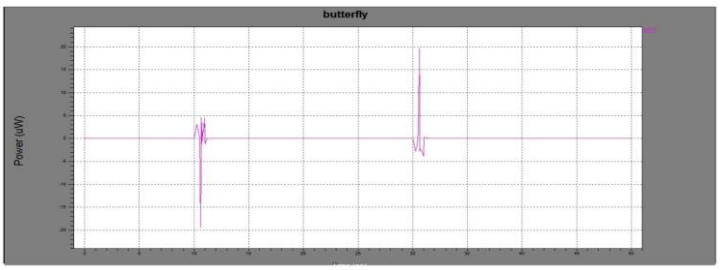

Fig 5.2(c) power analysis of butterfly ML scheme

Figure 5.2(c) shows the power analysis of butterfly ML TCAM employing TCAM structure of Asymmetric TCAM cell model. Due to this butterfly connection style, the circuit has got high degree of parallelism since it can do search operation of all TCAM cells at a time. Hence because of this power of this circuit has been reduced when compared to the conventional TCAM cell. And

obtained power is 19.7µW. and butterfly ML technique is reduce power is 85.29% and delay is 31.97% compared to conventional TCAM.

Table 5.1: TABULATED RESULTS

Proposed Configuration	**Power (µW)**	**Speed(Secs)**	**Power reduced compare to TCAM**	**Speed increased compare to TCAM**
Conventional TCAM Circuit	134	1.97		
Butterfly Match Line Scheme	19.7	1.34	85.29%	31.97%

VI. Conclusions

An energy efficient ternary content addressable Memory design is proposed in this paper. The reduction of high power consumption and delay which are the limiting factors of TCAM has been achieved by butterfly match line technique which is implemented in 0.18µm CMOS technology. The Butterfly match line technique is designed which is reduced power up to 88.29% and increased speed up to 31.97% compared to Conventional TCAM.

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